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Data Digitization and Fluorescence Signal Recognition for Telescope Array Experiment

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We have developed and made a test run of the Telescope Array (TA) Fluorescence Detector (FD) electronics. In this paper, we introduce TAFD signal processing and the method of separation of fluorescence and night sky back ground light, especially signal digitizing and one photomultiplier tube (PMT) level signal recognition board, we call as Signal Digitizer and Finder (SDF).

1. Introduction

In our Universe, Extraordinary High Energy Cosmic Rays (EHECRs), over 10^{20}eV, exist. And some of them reach to the earth [1]. The main themes of TA experiment are, precise extrapolating the energy and the arrival direction of each EHECR and obtaining the energy spectrum of them. Our experiment uses mainly two types of detector, one is called as Surface Detector (SD) and the other is FD.

We will distribute 576 SDs in 1.2 km mesh and total covering area will be 760 km^2. Each SD is two layer of plastic scintillator of 3 m^2 area and 1.2 cm thickness. The scintillation light is collected to PMT using wavelength shifting fiber. SD detects air shower particle directly.

Figure 1. FD station (left), mirror (middle), PMT camera with pre-amplifier (right) for fluorescence measurement.

FD measures the UV fluorescence of molecular nitrogen generated by air shower particles. One FD station (See Fig 1 left) has 12 pairs of segment mirrors and PMT cameras. Total field of view of each FD station is 3° to 34° in the elevation angle and 120° in the azimuth angle. The separation of each station is 30 to 40 km. We have installed 1st FD stations and 2 pairs of mirror and camera on this summer. The segment mirror (See Fig 1 middle) is 3.3 m diameter and composed of 18 hexagonal mirrors. The PMT camera (See Fig 1 right) is composed of 16x16 2-inch hexagonal PMTs, each camera covers 18.0°x15.5° patch of the sky and each

PMT pixel covers 1.1°x1.0°. Blue glass filter is mounted on PMT's photocathode for reduction of night sky background light and acrylic window is placed in front of camera for protect from dust.

2. Overview of FD electronics

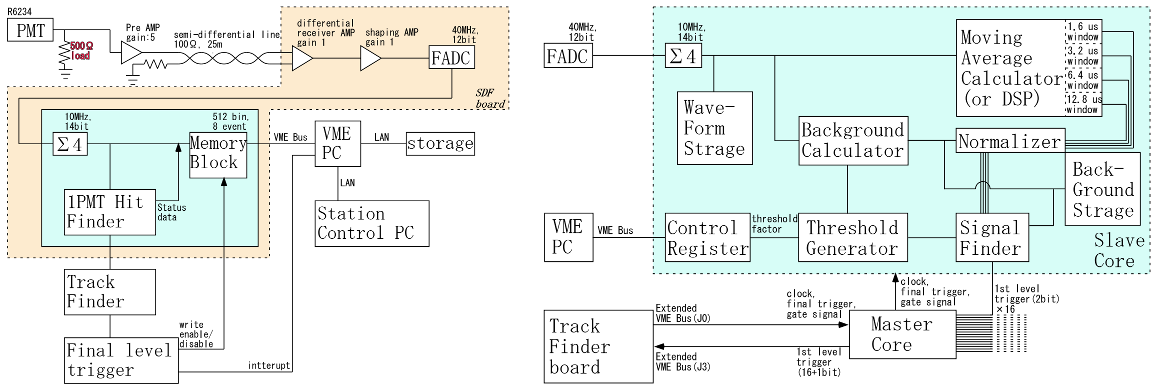

Figure 2. dataflow diagram of FD (left) and diagram of the 1 PMT level fluorescence signal recognition process (right).

2.1 Analog block

Operation gain of PMT will be set to 8×10^4, and PMT is DC coupled. A load reactance of PMT charge is 500 Ω and the voltage signal from the load reactance is amplified by a factor 5 with a pre-amplifier attached at the PMT head. Pre-amplifier output is 100 Ω semi-differential, and is sent to SDF though patch panel and 25 m cable.

SDF receives 16 semi-differential signals with receiver-amplifier and stretches the signal with waveform-shaping-amplifier(WFSA), to reduce the digital aliasing error and to filter out the background analog noise. WFSA is 2nd order integration low-pass-filter and time constant (TC) is 50 ns, the response function of WFSA is $\frac{t\exp(-t/TC)}{TC^2}$ and its gain is 1. TC value is chosed to make the integral eliasing error less than 1.0×10^{-3}. Output of WFSA is supplied into a 12-bit, 40 MHz Flash Analog Digital Converter (FADC). Maximum range of FADC is 2V, so least significant bit of FADC is equivalent to $2/2^{12}\simeq$0.5 mV. And all 16 outputs of WFSA is also supplied into a summation amplifier, it works as a low gain channel. The gain of the summation amplifier is 1/16. Output of the summation amplifier is sent to FADC, too.

2.2 Digital block

The digitized signal, from FADC for the WFSA, is sent to a Field Programmable Gate Array (FPGA), we call as the slave core. And The digitized signal, from FADC for the summation amplifier, is sent to another FPGA, called as the master core. The slave core signalprocesses and stores the digitized waveform of WFSA, recognizes the fluorescence signal, and send the result of signal recognition to another FPGA for board control, we call the master core. The slave core, at first, sum up 4 adjacent time slice for saving memory. So basic data become 14-bit, 10 MHz. We call this basic data as SUM4 count. The slave core has 8 event buffers thus causing no dead time to the DAQ system. The master core mainly stores the digitized waveform of the summation apmlifier, generates test pulse for debugging and transfers the result of signal recognition to the fluorescence track pattern recognition board, we call as Track Finder (TF). TF does the 1 camera level signal recognition, and sends the result to FD station control unit, we call as Central Trigger Distributor (CTD). CTD judges the result from TF, and distributes trigger to all modules in the FD station. Especially, the inter-mirror fluorescence track pattern recognition is done by CTD. CTD also distributes clock and reset signal, and stores the time stamp information from a global positioning system unit on itself.

SDF, TF, CTD are all VME 9U modules, and have two types extended VME-bus. We call, one as KEKJ0, and the others as J3. KEKJ0 is used for ± 3.3V , -5V DC power supply and the transfer clock, reset, trigger, and control signal from TF to SDF. J3 is used for the transfer the result of the 1 PMT level signal recognition from SDF to TF.

All of fluorescence signal recognizing processes are made in successive pipeline every 12.8 μs. And all processes are done in the digital logic circuit. We will introduce the detail of 1 PMT level fluorescence signal recognizing process in the next section. The detail of TF and CTD will be reported by our colleague in this conference.

3. Detail of SDF

3.1 Process of 1 PMT level signal recognition

The 1 PMT level fluorescence signal recognition in the slave core is as follows (See Figure 2):

1. Moving average in each time window of 0.8, 1.6, 3.2, 6.4, 12.8 μs are calculated. These time window widthes are optimized for maximazing S/N ratio.

2. Average and standard deviation are calculated from past 1.6 ms ,they are updated each 0.4 ms.

3. Moving average counts are normalized by them.

4. If the normalized counts are larger than threshold constants, the slave core interpret it as the fluorescence signal. Threshold constants are variable for each time window.

5. If any one of FADC was saturate, the slave core also interpret it as the fluorescence signal.

3.2 Main components of the SDF

One SDF processes 16 PMT imput and main components are follows (See Figure 3):
1. 16 pairs of the receiver amplifier and WFSA.
2. 1 summation amplifier.
3. 16+1 FADCs, 1 is for the summation amplifier, others are for WFSAs.
4. 8+1 FPGAs, 1 is for the master core. Eace one of other FPGAs has a couple of slave core.
5. 1 complex programmable logic device for VME interface.
6. 2 digital-to-analog converter for generating test pulse.
7. 2 NIM outputs and 4 NIM inputs, they can be used for any digital signals.

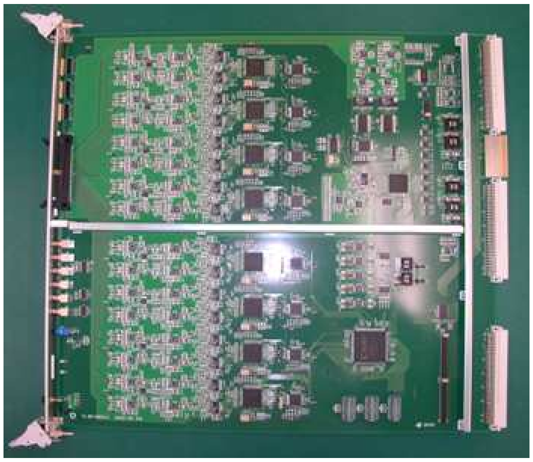

Figure 3. a picture of 2nd prototype SDF

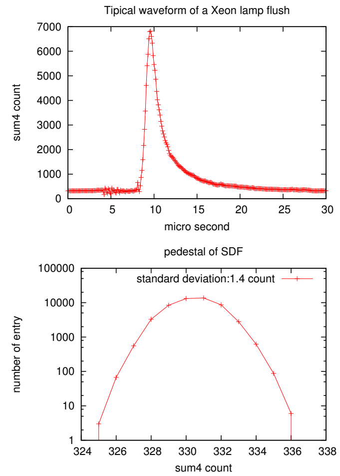

Figure 4. Tipical waveform (top) and pedestal of analog back gound noise (bottom) of SDF.

3.3 Basic performance of the SDF

1. The standard deviation of the analog back gound noise is typically 2 SUM4 counts, this value is equevalent to 0.25 mV,
2. The linearity error of DC input is less than 1.0×10^{-3}, and that of 25 ns width pulse is less than 1.0×10^{-2}.

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